III. REMARKS

Claims 1-22 are pending in this application. By this amendment, claims 1, 3, 8, 11, 16 and 18 have been amended. These amendments are being made to facilitate early allowance of the presently claimed subject matter. Applicants do not acquiesce in the correctness of the rejections and reserve the right to present specific arguments regarding any rejected claims not specifically addressed. Further, Applicants reserve the right to pursue the full scope of the subject matter of the original claims in a subsequent patent application that claims priority to the instant application. Reconsideration in view of the following remarks is respectfully requested.

Entry of this Amendment is proper under 37 C.F.R. 1.116(b) because the Amendment: (a) places the application in condition for allowance as discussed below; (b) does not raise any new issues requiring further search and/or consideration; and (c) places the application in better form for appeal. Accordingly, Applicants respectfully request entry of this Amendment.

In the Office Action, claim 1-22 are rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Chiu *et al.* (U.S. Patent No. 6,584,606 B1), hereafter "Chiu." Applicants assert that Chiu does not teach each and every feature of the claimed invention. For example, with respect to independent claims 1, 8 and 16, Applicants submit that Chiu fails to teach a control file that includes a proposed placement of a set of I/O pad groups on the chip, wherein each of the set of I/O pad groups includes at least one power pad. The Office equates the control file of the claimed invention with the proposed I/O design of Chiu that "...includes such characteristics as the designer's intended load on the I/O cells, the switching factor, I/O duty cycle, the temperature at which the design is proposed to operate, and a proposed operational lifetime in terms of thousands of power on hours (KPOH)." Col. 6, lines 16-20. The Office then cites a passage in

Chiu that discusses ASIC design with "...each chip being configured with wiring to supply ground and power connection to multiple I/O cell placement locations." Col. 1, lines 31-47. To this extent, Chui teaches a proposed I/O design and that each chip has power connection, but does not indicate that its I/O cells in the proposed I/O design are organized into I/O cell groups that each include at least one power connection.

In contrast, the claimed invention includes "...a control file that includes a proposed placement of a set of I/O pad groups on the chip, wherein each of the set of I/O pad groups includes at least one power pad." Claim 1. As such, the control file of the claimed invention does not merely teach power connection in isolation from an proposed I/O design as does Chiu, but rather includes a proposed placement of a set of I/O pad group on the chip, wherein each of the set of I/O pad groups includes at least one power pad. Thus, the proposed I/O design that is used as input in the Chiu does not teach the control file of I/O pad groups that each include at least one power pad of the claimed invention. Accordingly, Applicants respectfully request that the Office withdraw its rejection.

With further respect to independent claims 1, 8, and 16, Applicants respectfully submit that Chiu also fails to teach a calculation system for calculating a group switching current of a particular I/O pad group identified in the control file based on individual switching currents of each I/O pad in the particular I/O pad group, and for comparing the group switching current to a predetermined maximum switching current. As stated above, Chiu does not group its I/O cells in groups each having at least one power pad in its proposed I/O design. As such, Chiu does not have the ability to make a calculation and comparison based on such a I/O pad group. Furthermore, the passages of Chiu cited by the Office teach in isolation that a solver calculates

currents *for each I/O cell*; that a proposed placement of one I/O cell may affect other cells, as groups of cell placement slots may be supplied by the same power distribution wiring; and a table in which cells are members of groups for purposes of checking the associated limit such as EM and di/dt noise. Col. 6, lines 51+; col. 6, lines 12-15; Table 1; col. 9, lines 35-47. However, Chiu teaches only that its solver calculates currents *for each cell* and not for a group of cells having at least one power cell. Furthermore, even though Chiu acknowledges power limits causing the placement of an I/O cell to affect other I/O cells in a group, Chiu never teaches that its checking program specifically checks for this, but instead for IR voltage drop, electromigration (EM) limits, and noise limit rules. See col. 5, lines 42-55; col. 6, lines 55+. Still further, the LIM1, LIM2 and LIM3 limits specified by Chiu in Table 1 and described in col. 9, lines 40-59 as cited by the Office, do not describe limits of the switching current of a group, but only "...a parameter, such as EM and di/dt noise." Col. 9, lines 38-39. Thus, the three disparate citations of the Office do not teach calculating of a group switching current.

The Office further argues this feature of the claimed invention is taught by a passage of Chiu, which teaches "...'the limit for all members of group I001 ... for the GRP3/LIM3 di/dt noise checking ("group switching current") is 800milliAmps/nanosecond.'" Office Action, page 8. To this extent, the Office equates the group switching current of the claimed invention with the di/dt noise checking of Chiu. However, as is well known in the art noise is an unwanted signal that invades the electrical signal. See Exhibit A. As such, di/dt noise is not equivalent to switching current, e.g. the current supplied from a power pad. Thus, nowhere in the passage cited by the Office or elsewhere does Chiu teach calculating group switching current.

The claimed invention, in contrast, includes "...a calculation system for calculating a group switching current of a particular I/O pad group identified in the control file based on individual switching currents of each I/O pad in the particular I/O pad group, and for comparing the group switching current to a predetermined maximum switching current." Claim 1. As such, the calculation system of the claimed invention, rather than determining factors such the di/dt noise as does Chiu, instead calculates a group switching current of a particular I/O pad group. Furthermore, unlike the separate calculation of currents for each I/O cell; the affecting of cells by placement of a cell; and table having groups of cells of Chiu, the calculating and comparing of the claimed invention is to a predetermined maximum switching current and for a particular I/O pad group identified in the control file. For the above reasons, the calculation system of the claimed invention is not taught by Chiu. Accordingly, Applicants request that the rejection be withdrawn.

With regard to newly amended claims 3, 11and 18, Applicants submit that the cited references do not teach or suggest each and every feature of the claimed invention. For example, Chiu does not teach that each of the set of I/O pad groups in the control file includes one power pad. Accordingly, Applicants submit that the claims are in condition for allowance.

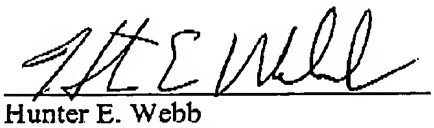
With regard to the Office's other arguments regarding dependent claims, Applicants herein incorporate the arguments presented above with respect to independent claims listed above. In addition, Applicants submit that all dependant claims are allowable based on their own distinct features. However, for brevity, Applicants will forego addressing each of these rejections individually, but reserve the right to do so should it become necessary. Accordingly, Applicants respectfully requests that the Office withdraw its rejection.

IV. CONCLUSION

In addition to the above arguments, Applicants submit that each of the pending claims is patentable for one or more additional unique features. To this extent, Applicants do not acquiesce to the Office's interpretation of the claimed subject matter or the references used in rejecting the claimed subject matter. These features have not been separately addressed herein for brevity. However, Applicants reserve the right to present such arguments in a later response should one be necessary.

In light of the above, Applicants respectfully submits that all claims are in condition for allowance. Should the Examiner require anything further to place the application in better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the number listed below.

Respectfully submitted,



Date: February 28, 2006

Hunter E. Webb
Reg. No.: 54,593

Hoffman, Warnick & D'Alessandro LLC
75 State Street, 14th Floor
Albany, New York 12207
(518) 449-0044
(518) 449-0047 (fax)

RAD/hew

EXHIBIT A

TechWeb
The Business Technology Network

TechEncyclopedia More than 20,000 IT terms

Results found for: noise

noise

An extraneous, unwanted signal that invades an electrical or optical system. In electronics, noise can come from strong electrical or magnetic signals in nearby lines, from poorly fitting electrical contacts and from power line spikes. In optics, noise comes from the stray reflections of light that emanate from the various components in the optical system. See signal-to-noise ratio and noise cancellation.

TERMS SIMILAR TO YOUR ENTRY

Entries before noise

- nodal processing delay
- node
- node address
- node tree
- no execute

Entries after noise

- noise cancellation
- NOMAD
- nomadic computing
- NOMDA
- NOME

DEFINE ANOTHER IT TERM

Define

Or get a random definition